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Docket No. SEC.636
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TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE

and invented by:

Won-Suk YANG
Ki-Nam KIM
Chang-Hyun CHO

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

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Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having **25** pages and including the following:

   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 16
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4. ☒ Oath or Declaration
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   c. ☒ With Power of Attorney ☐ Without Power of Attorney
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   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
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   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
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15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

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CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	19	- 20 =	0	x	$18.00	$0.00
Indep. Claims	2	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
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Brian C Altmiller

Signature

Dated: **MAY 18, 1999**

BRIAN C. ALTMILLER
REG. NO. 37,271

JONES VOLENTINE, L.L.P.
12200 SUNRISE VALLEY DRIVE, SUITE 150
RESTON, VA 20191

TEL. NO. (703) 715-0870

cc:

METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE

This application relies for priority upon Korean Patent Application No. 98-18167, filed on May 20, 1998, the contents of which are herein incorporated by reference in their entirety.

Field of the Invention

The present invention relates to a semiconductor device and a method of manufacturing such a device. More particularly, the present invention relates to a method for fabricating a MOS transistor having gate double sidewall spacers.

Background of the Invention

A DRAM cell device is generally divided into a cell array region and a peripheral logic region. The cell array region includes a plurality of memory cells in a matrix-type format, and the peripheral region includes a circuit to operate the memory cells.

Transistors are formed in both the cell array region and in the peripheral region, respectively, to have different optimal characteristics, since the transistors must function differently according to their roles in the device. For example, the transistor in the cell array region may have a single source/drain region made of a low concentration impurity diffusion region, while a transistor in the peripheral region may have a source/drain of a LDD (lightly doped drain) structure. In addition, the transistor in the cell array region

may have gate single spacers and the transistor in the peripheral region may have gate double spacers.

Figs. 1A to 1C are cross-sectional views of MOS transistors formed by a conventional method. Fig. 1A schematically shows a cell array NMOS transistor in a cell array region. Referring to Fig. 1A, the cell array NMOS transistor includes a gate electrode 12 formed over a semiconductor substrate 10, gate spacers 14, with a thickness of about 700Å to 800Å, aligned on either lateral side of the gate electrode 12, and a low concentration n-type impurity diffusion region 16 with a predetermined depth in the semiconductor substrate 10, outwardly disposed from the gate spacers 14.

Figs. 1B and 1C schematically show a peripheral NMOS transistor and a peripheral PMOS transistor, respectively, formed on the peripheral region. The peripheral NMOS transistor includes a gate electrode 22, gate spacers 24, with a thickness of about 700Å to 800Å, aligned on either lateral side of the gate electrode 22, a low concentration n-type impurity diffusion region 25 with a predetermined depth, in the semiconductor substrate 10, downwardly disposed from lateral edge of the gate spacers 24, and a high concentration n-type impurity region 26 with a predetermined depth in the semiconductor substrate 10, disposed outwardly from a lateral edge of the gate spacers 24. In other words, the peripheral NMOS transistor has a so-called LDD (lightly doped drain) structure.

Referring to Fig. 1C, the peripheral PMOS transistor includes a gate electrode 32, gate spacers 34, with a thickness of about 700Å to 800Å, aligned on lateral side of the

gate electrode 32, a low concentration n-type or p-type impurity diffusion region 35, with a predetermined depth in the semiconductor substrate 10 downwardly disposed from a lateral edge of the gate spacers 34, and a high concentration p-type impurity region 36, with a predetermined depth in the semiconductor substrate 10 disposed outwardly from lateral edge of the gate spacers 34. In other words, the peripheral PMOS transistor also has a so-called LDD (lightly doped drain) structure.

The n-type impurity preferably comprises P (phosphorous), As (arsenic), or the like. As is well known, an arsenic impurity has a greater molecular weight than a phosphorous impurity and can therefore cause substrate damage and current leakage. On the other hand, phosphorous has a greater diffusion rate than arsenic and can therefore cause a short channel effect in the transistor. As a result, phosphorous is generally used for the formation of transistors in the cell array region, for clear on/off operation and improved refresh time. In the peripheral region, phosphorous is generally used for long channel transistors, and arsenic is generally used for short channel transistors, despite the danger of leakage loss.

As described above, phosphorous ions have a greater diffusion rate, which increases the short channel effect. To address problems with phosphorous ions and to obtain a maximum effective channel length, cell array NMOS transistors in the cell array region are formed according to the following process sequence. After a gate spacer 24 is formed on the lateral sidewall of the gate 22, an impurity ions implanting process is performed using the gate 22 and gate spacer 24 as a mask, to form an n-type impurity

diffusion region 26 and thereby obtain a maximum effective channel length. A heat treatment is required, however, to drive out n-type impurities into the semiconductor substrate both outside of the gate electrode. It is very difficult, however, to diffuse out n-type impurities to a desired depth within the semiconductor substrate.

Also, the impurity in the peripheral region simultaneously diffuses out and the effective channel length of the transistor is likewise reduced, thereby causing the device fail. In particular, a p-type impurity diffusion region of the peripheral PMOS transistor in the peripheral region is formed by implanting boron (B), which has a greater diffusion rate. As a result, the peripheral PMOS transistor is greatly affected by the reduction of the effective channel length.

To address the effect of the reduced effective channel length in the peripheral region, an n-type low-concentration impurity diffusion region can be replaced by a different n-type low concentration impurity diffusion region as shown in Fig. 1C. By doing this, the problem of reduction of the effective channel length encountered in the p-type diffusion region can be prevented. As can be seen in Fig. 1C, a high concentration p-type impurity diffusion region is overlapped with low concentration n-type impurity diffusion region. However, the formation of such diffusion region configuration requires very careful controlling of both the thickness of the gate spacer 34 and of the annealing temperature. Also, the diffusion of a high concentration p-type impurity makes the impurity in the LDD region maintain a high concentration, thus making it difficult to prevent hot carrier effect.

Summary of the Invention

The present invention was made in view of the above problem, and it is therefore an object of the invention to provide a MOS transistor with an improved source/drain structural configuration, as well as a method for fabricating a MOS transistor that can prevent a short channel effect and a hot carrier effect and can avoid a reduction in the effective channel length.

The present invention provides for a double LDD structure comprising a first lightly-doped region of first type, a second lightly-doped region of second type, and a third heavily-doped region of second type. Such a double LDD structure in accordance with the present invention is formed by first implanting a low concentration of an impurity of a first type into a semiconductor substrate using a gate as a mask. Second implantation of a low concentration of an impurity of a second type is implemented after the formation of first gate spacers on lateral sides of the gate. After the second implantation, second gate spacers are formed adjacent to the first gate spacers, and a third implantation of a high concentration of an impurity of a second type is implemented using the double gate spacers as a mask. Implanted impurities are then diffused out by a heat treatment and so complete the LDD structure.

In accordance with one aspect of the present invention, the method for fabricating a MOS transistor includes forming a device isolation region on a semiconductor substrate to define a cell array region and a peripheral circuit region, forming a first gate in the cell array region, a second gate in the peripheral circuit region, and a third gate in the

peripheral circuit region, implanting first impurity ions of a low concentration into a first portion of the semiconductor substrate adjacent to the second and third gates, using the second and third gates as a mask, to form a first impurity diffusion region of a first conductivity type, forming first gate spacers on lateral sides of the first, second, and third gates, implanting second impurity ions of a low concentration into a second portion of the semiconductor substrate adjacent to the first gate and first gate spacers, using the first gate and first gate spacers as a mask, to form a second impurity diffusion region of a first conductivity type, implanting third impurity ions of a low concentration into a third portion of the semiconductor substrate adjacent to the third gate and first gate spacers, using the third gate and first gate spacers as a mask, to form a third impurity diffusion region of a second conductivity type, forming an insulating layer over the semiconductor substrate, first through third gates, and first gate spacers, etching the insulating layer in the peripheral region to form second gate spacers adjacent to the first spacers adjacent to the second and third gates, implanting fourth impurity ions of a high concentration into a fourth portion of the semiconductor substrate adjacent to the second gate and second spacers, using the second gate and first and second spacers as a mask, to form a fourth impurity diffusion region of a first conductivity type, and implanting fifth impurity ions of a high concentration into a fifth portion of the semiconductor substrate adjacent to the third gate and second spacers, using the third gate and first and second spacers as a mask, to form a fifth impurity diffusion region of a second conductivity type.

In accordance with another aspect of the present invention, the method for fabricating a MOS transistor includes forming a gate electrode over a semiconductor substrate, implanting first impurity ions at a low concentration of a first conductivity type, using the gate electrode as a mask, to form a first impurity diffusion layer, forming first spacers on lateral sides of the gate, implanting second impurity ions at a low concentration of a second conductivity type, using the gate and first spacers as a mask, to form a second impurity diffusion layer, forming a second spacers adjacent to the first spacers, implanting third impurity ions of high concentration of a second conductivity type, using the gate and the first and second spacers as a mask, to form a third impurity diffusion layer, and annealing and diffusing the impurity diffusion layers to overlap the first diffusion layer with the second diffusion layer.

Brief Description of the Drawings

These and other features, aspects, and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings where:

Figs. 1A to 1C illustrate cross-sectional views of completed MOS transistor configurations manufactured in accordance with a conventional method;

Figs. 2A to 2C illustrate cross-sectional views of a semiconductor substrate having a gate electrode wherein an implantation of a low concentration of n-type impurities is

carried out only in the peripheral region in accordance with a preferred embodiment of the present invention;

Figs. 3A to 3C respectively illustrate a process step subsequent to that shown in Figs. 2A to 2C, wherein first gate spacers are formed on sidewalls of the gate electrode;

Figs. 4A to 4C respectively illustrate a process step subsequent to that shown in Figs. 3A to 3C, wherein an implantation of a low concentration of n-type impurities is carried out only in the cell array region, using the first spacers and gate electrode as a mask;

Figs. 5A to 5C respectively illustrate a process step subsequent to that shown in Figs. 4A to 4C, wherein an implantation of a low concentration of p-type impurities is carried out in the peripheral region;

Figs. 6A to 6C respectively illustrate a process step subsequent to that shown in Figs. 5A to 5C, wherein an insulating layer for use as second spacers is formed;

Figs. 7A to 7C respectively illustrate a process step subsequent to that shown in Figs. 6A to 6C, wherein an etch back is carried out only in the peripheral region to form second spacers on sidewalls of the first spacers in the peripheral region;

Figs. 8A to 8C respectively illustrate a process step subsequent to that shown in Figs. 7A to 7C, wherein an implantation of a high concentration of n-type impurities is carried out only in the peripheral region;

Figs. 9A to 9C respectively illustrate a process step subsequent to that shown in Figs. 8A to 8C wherein an implantation of a high concentration of p-type impurities is carried out only in the portion of the peripheral region containing peripheral PMOS transistors, for PMOS transistor formation in the peripheral region;

Figs. 10A to 10C respectively illustrate a process step subsequent to that shown in Figs. 9A to 9C wherein a silicidation process is carried out to form a silicide layer in the peripheral region; and

Figs. 11A to 11 respectively illustrate a process step subsequent to that shown in Figs. 10A to 10C wherein a contact hole is formed in the cell array region.

Detailed Description of the Preferred Embodiments

In keeping with the objects of the invention, a method for fabricating a MOSFET device is covered in detail with reference to accompanying drawings. The present invention is particularly related to a MOS transistor with a double LDD structure, especially the forming of a PMOS transistor with a double LDD structure in a peripheral region of a memory device, while forming an NMOS transistor with a single LDD structure in a cell array region. The double LDD structure of PMOS in the peripheral region acts to suppress both a short channel effect and a hot carrier effect.

Figs. 2A to 11A illustrate, at selected stages of fabrication, the cross-sections of a cell array NMOS transistor in the cell array region in accordance with a preferred embodiment of the present invention; Figs. 2B to 11B illustrate, at selected stages of

fabrication, the cross-sections of a peripheral NMOS transistor in the peripheral region in accordance with a preferred embodiment of the present invention; and Figs. 2C to 11C illustrate, at selected stages of fabrication, the cross-sections of a peripheral PMOS transistor in the peripheral region in accordance with a preferred embodiment of the present invention.

Referring to Figs. 2A to 2C, a device isolation layer (not shown) is formed in a semiconductor substrate 100 to define a cell array region and a peripheral region, and a gate oxide layer (not shown) is formed over the semiconductor substrate 100. Gate electrodes are then simultaneously formed in the cell array region (Fig. 2A) and in the peripheral region (Fig. 2B and Fig. 2C), i.e., a first gate electrode 102a, a second gate electrode 102b, and a third gate electrode 102c are formed. The gate electrodes 102a, 102b, and 102c are preferably formed by depositing and patterning a polysilicon layer over the substrate 100.

Since the cell array region is more susceptible to the design rule than the peripheral region, gate widths in the cell array region must be narrower than those in the peripheral region. This can be seen on Figs. 2A-2C by comparing the width of the gate electrode in Fig. 2A with those in Figs. 2B and 2C.

After the formation of the gate electrodes 102a-102c, a first photoresist layer (not shown) is formed, preferably by spin coating, over the semiconductor substrate 100 and the first gate electrode 102a, and is patterned into a desired configuration, i.e., first photoresist pattern 103, exposing the peripheral region while covering the cell array

region. Low concentration n-type impurity ions are then implanted into the semiconductor substrate 100 of the peripheral region using the gate electrodes 102b and 102c as a mask, thereby forming first, n-type impurity diffusion layers 104b and 104c, respectively. The implantation of n-type impurity ions is preferably carried out with arsenic (As) at an energy of about 50keV, with a dose of about $5x10^{12}$ ions/cm^2.

The formation of first spacers is next addressed and shown schematically in Figs. 3A to 3C. After removing the first photoresist pattern 103, a first insulating layer, e.g., a silicon nitride layer, (not shown) is deposited over the entire resulting semiconductor topology. The deposited insulating layer is then anisotropically etched to form first gate spacers 106a, 106b, and 106c on the sidewalls of the first, second, and third gate electrodes 102a-102b, respectively, preferably with a thickness of about 400Å.

The next process sequence is the formation of a low concentration n-type impurity diffusion layer in the cell array region. Referring to Figs. 4A to 4C, a second photoresist layer (not shown) is deposited, preferably by spin coating, over the entire resulting semiconductor topology and is patterned into the desired configuration, i.e., a second photoresist pattern 107 exposing the cell array region while covering the peripheral region. Low concentration n-type impurity ions are then implanted into the semiconductor substrate 100 in the cell array region using the gate electrode 102a and the first spacers 106a as a mask. This results in the formation of a second, n-type impurity diffusion layer 108a in the cell array region. This implantation is preferably carried out

using phosphorous (P) ions at an energy of about 30keV, with a dose of about $5x10^{12}$ ions/cm^2.

After removing the second photoresist pattern 107, a third photoresist layer (not shown) is then deposited and patterned into a desired configuration, i.e., a third photoresist pattern 109. The third photoresist pattern 109 exposes only the third gate electrode 102c in the peripheral region where a peripheral PMOS transistor is to be formed, as shown in Figs. 5A to 5C. At this point, the first gate electrode 102a and the second gate electrode 102b are covered by the third photoresist pattern 109. Low concentration p-type impurity ions are then implanted into the semiconductor substrate 100 in the peripheral region using the third gate electrode 102c and the first spacers 106c as a mask, to thereby form a third, p-type impurity diffusion layer 110c of in the cell array region. The p-type impurity may include boron (B) or BF_3 and these impurity ions are preferably implanted at an energy of about 20keV, with a dose of about $1x10^{13}$ ions/cm^2.

Referring to Figs. 6A to 6C, after removing the third photoresist pattern 109, an insulating layer 112, e.g., a silicon nitride layer, is deposited over the resulting semiconductor topology. As will be described later, the insulating layer 112 serves as a barrier layer against silicidation in the cell array region and also serves to facilitate the formation of second gate spacers in the peripheral region.

A fourth photoresist layer (not shown) is then deposited and patterned into a desired configuration, i.e., a fourth photoresist pattern 111. The fourth photoresist pattern 111 exposes the insulating layer 112 in the peripheral region while covering the insulating

layer 112 in the cell array region. As shown in Figs. 7A to 7C, the insulating layer 112 is then anisotropically etched, using the fourth photoresist pattern 111 as a mask, to respectively form second spacers 112b and 112c adjacent to the first spacers 106b and 106c by the second and third gate electrodes 102b and 102c, with a thickness of about 400Å.

As a result of this etching, a double spacer configuration is formed next to the gates in the peripheral region. At this point, because the insulating layer 112 in the cell array region is covered by the fourth photoresist pattern 111, it is not etched, and a portion of the insulating layer 112 remains in the cell array region. This remaining insulating layer 112a will serve as a barrier layer against silicidation.

After removing the fourth photoresist pattern 111, a fifth photoresist layer (not shown) is then deposited and patterned into a desired configuration, i.e., a fifth photoresist pattern 113. As shown in Figs. 8A to 8C, the fifth photoresist pattern 113 is formed to expose only the second gate electrode 102b and its spacers 106b and 112b in the peripheral region, while covering the first and third gate electrodes 102a and 102c and their spacers 106a, 106c, and 112c. Using the fifth photoresist pattern 115, the gate electrode 102b, and the second and third spacers 106b and 112b as a mask, high concentration n-type impurity ions are implanted into the semiconductor substrate 100 to form a fourth, n-type impurity diffusion layer 114c. The implantation of n-type impurity ions is preferably carried out using arsenic (As) at an energy of about 20keV, with a dose of about $5x10^{15}$ ions/cm^2.

After removing the fifth photoresist pattern 113, a sixth photoresist layer (not shown) is then deposited and patterned into a desired configuration, i.e., a sixth photoresist pattern 115. As shown in Figs. 9A to 9C, the sixth photoresist pattern 115 is formed to expose only the region where the peripheral PMOS transistor is to be formed, i.e., to expose the third gate electrode 102c and spacers 106c and 112c. Using the sixth photoresist pattern 115, the third gate electrode 102c, and the spacers 106c and 112c as a mask, high concentration p-type impurity ions are implanted into the semiconductor substrate 100 to form a fifth, p-type impurity diffusion layer 116c in the peripheral region. The p-type impurity preferably includes boron (B) or BF_3 and these impurity ions are preferably implanted at an energy of about 20 keV, with a dose of about $5x10^{15}$ ions/cm^2. Consequently, a peripheral PMOS transistor is formed in the peripheral region to the desired configuration with a first impurity diffusion layer 104c of a low concentration n-type impurity, a third impurity diffusion layer 110c of a low concentration p-type impurity, and a fifth impurity diffusion layer 116c of a high concentration p-type impurity.

The next process sequence is the formation of the silicide layer, which is schematically shown in Figs. 10A to 10C. A silicide layer formed over the source/drain region and over the gate electrodes in the peripheral region can decrease the consumption voltage of the resulting DRAM device and can increase its operation speed. At this point, a transition metal, such as Ti, Ta, Co, or Mo, is deposited over the resulting

semiconductor topology as a transition metal layer (not shown). After depositing the transition metal, an annealing process is carried out to form a silicide layer 118.

As is well known, the silicide layer 118 is formed by the reaction between silicon and the transition metal. Therefore, as can be seen in Figs.10B and 10C, the silicide layer 118 is formed only on areas of exposed silicon and polysilicon, i.e., on the exposed semiconductor substrate 100 and on the exposed polysilicon gates 102b and 102c in the peripheral region. Because the remaining insulating layer 112a covers the semiconductor substrate and the first gate electrode in the cell array region no silicidation occurs in the cell array region. The presence of the remaining insulating layer 112a prevents the silicidation process in the cell array region by preventing the transition metal from contacting any silicon. Were this not prevented, the current leakage of the transistors in the cell array region would be undesirably increased.

During the annealing process for silicidation, impurity ions of the previously mentioned impurity diffusion layers are diffused to form respective impurity regions. More specifically, referring to Figs. 10A to 10C, the transistor formed on the cell array region, i.e., the cell array NMOS transistor (see Fig. 10A), includes the first gate electrode 102a, first spacers 106a, and a source/drain region 108a (i.e., the second impurity region 108a) of a low concentration n-type impurity. The NMOS transistor formed on the peripheral region, i.e., the peripheral NMOS transistor (see Fig. 10B) includes the second gate electrode 102b, first and second spacers 106b and 112b, and source/drain regions 104b and 114b. As can be seen, the source/drains comprise the first impurity region 104b

of a low concentration n-type impurity aligned below the first and second spacers 106b and 112b and the fourth impurity region 114b of a high concentration n-type impurity aligned outwardly from the lateral edges of the second spacers 112b. The PMOS transistor formed on the peripheral region, i.e., the peripheral PMOS transistor (see Fig. 10C) includes the third gate electrode 102c, first and second spacers 106c and 112c, and source/drain regions 104c, 110c, and 116c. As can be seen in Fig. 10C, the source/drain regions comprise the first impurity region 104c of low concentration n-type impurity, aligned below the first spacers 106c, the third impurity region 110c of low concentration p-type impurity, aligned below the second spacers 112c, and the fifth impurity region 116c of high concentration p-type impurity, aligned outwardly from the lateral edges of the second spacers 112c.

In the peripheral PMOS transistor, the heat burden applied to the semiconductor device during subsequent layer formation processes makes the first impurity region 104c of n-type overlap with the third impurity region 110c and thereby transforms the first impurity region 104c from n-type to p-type.

After the formation of the silicide layer, a remaining portion of the transition layer which has not reacted with the silicon or polysilicon is removed. As a result, the sheet resistance of the source/drain region can be reduced to increase the operation speed of the device.

Referring to Figs. 11A to 11C, an interlayer insulating layer 120 is then deposited over the entire semiconductor substrate. A seventh photoresist layer (not shown) is

deposited over the interlayer insulating layer and is patterned into a desired configuration. Using the seventh photoresist pattern (not shown), desired portions of the interlayer insulating layer 120 are anisotropically etched to form a contact hole that exposes the source/drain region of the cell array NMOS transistor, as shown in Fig. 11A. The interlayer insulating layer 120 is selectively etched (preferably for about five times) with respect to the remaining insulating layer 112a and thereby forms the contact hole in a self aligned manner.

According to the present invention, the cell array NMOS transistor includes a gate electrode, a single spacer, and a source/drain region of low concentration n-type impurity region. The peripheral NMOS transistor includes a gate electrode, double spacers, and an LDD source/drain region including a low concentration n-type impurity region and a high concentration n-type impurity region. The peripheral PMOS transistor includes a gate electrode, double spacers, and a double LDD source/drain structure including a low concentration p-type impurity region, a low concentration n-type impurity region, and a high concentration p-type impurity region. The double LDD source/drain structure of the peripheral PMOS transistor can prevent the short channel effect and can reduce the hot carrier effect. Furthermore, the remainder of the insulating layer used to create the second spacers serves the additional purpose of being a silicidation barrier layer and etching stopping layer and thereby simplifies the manufacturing process.

It will be recognized by those skilled in the art that the innovative concepts disclosed in the present application can be applied in a wide variety of contexts. Moreover, the preferred implementation can be modified in a tremendous variety of ways. Accordingly, it should be understood that the modification and variations suggested below and above are merely illustrative. These examples may help to show some of the scope of the inventive concepts, but these examples are not intended to exhaust the full scope of variation in the disclosed novel concepts.

WHAT IS CLAIMED IS :

1. A method for fabricating a semiconductor device comprising:

forming a device isolation region on a semiconductor substrate to define a cell array region and a peripheral circuit region;

forming a first gate in the cell array region, a second gate in the peripheral circuit region, and a third gate in the peripheral circuit region;

implanting first impurity ions of a low concentration into a first portion of the semiconductor substrate adjacent to the second and third gates, using the second and third gates as a mask, to form a first impurity diffusion region of a first conductivity type;

forming first gate spacers on lateral sides of the first, second, and third gates;

implanting second impurity ions of a low concentration into a second portion of the semiconductor substrate adjacent to the first gate and first gate spacers, using the first gate and first gate spacers as a mask, to form a second impurity diffusion region of a first conductivity type;

implanting third impurity ions of a low concentration into a third portion of the semiconductor substrate adjacent to the third gate and first gate spacers, using the third gate and first gate spacers as a mask, to form a third impurity diffusion region of a second conductivity type;

forming an insulating layer over the semiconductor substrate, first through third gates, and first gate spacers;

etching the insulating layer in the peripheral region to form second gate spacers adjacent to the first spacers adjacent to the second and third gates;

implanting fourth impurity ions of a high concentration into a fourth portion of the semiconductor substrate adjacent to the second gate and second spacers, using the second gate and first and second spacers as a mask, to form a fourth impurity diffusion region of a first conductivity type; and

implanting fifth impurity ions of a high concentration into a fifth portion of the semiconductor substrate adjacent to the third gate and second spacers, using the third gate and first and second spacers as a mask, to form a fifth impurity diffusion region of a second conductivity type.

2. A method for fabricating a semiconductor device, as recited in claim 1, wherein the first conductivity type is n-type.

3. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of first impurity ions has a lower ion diffusivity than the step of implanting second impurity ions.

4. A method for fabricating a semiconductor device, as recited in claim 1, wherein the first through third gates comprise polysilicon.

5. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of first impurity ions is performed using arsenic with a dose range of about $5x10^{12}$ ions/cm^2 and at an energy range of about 50 keV.

6. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of second impurity ions is performed using phosphorous with a dose range of about $5x10^{12}$ ions/cm^2 and at an energy range of about 30 keV.

7. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of third impurity ions is performed using boron or BF_3 with a dose range of about $1x10^{13}$ ions/cm^2 and at an energy range of about 20 keV.

8. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of fourth impurity ions is performed using arsenic with a dose range of about $5x10^{15}$ ions/cm^2 and at an energy range of about 50 keV.

9. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of fifth impurity ions is performed using boron or BF_3 with a dose range of about $5x10^{15}$ ions/cm^2 and at an energy range of about 20 keV.

10. A method for fabricating a semiconductor device, as recited in claim 1, further comprising:

forming a silicide layer over the semiconductor substrate, the second gate, and the third gate in the peripheral circuit region; and

forming an interlayer insulating layer over the substrate and first through third gates;

etching a selected portion of the interlayer insulating layer in the cell array region, using the insulating layer as for an etching stopper, and forming a contact opening adjacent to the first gate.

11. A method for fabricating a semiconductor device, as recited in claim 10, wherein the forming of a silicide layer is further comprises

forming a transition metal over the substrate and the second and third gates

annealing the substrate and the transition metal to form the silicide layer.

12. A method for fabricating a semiconductor device, as recited in claim 11, wherein during the annealing of the substrate and the transition ,metal, the first through fifth impurities are diffused into the first through fifth impurity diffusion regions, respectively.

13. A method for fabricating a semiconductor device, as recited in claim 10, wherein the a remaining portion of the insulating layer, after the etching of the insulating layer in the peripheral region, serves as a barrier layer to prevent silicidation in the cell array area during the forming of a silicide layer.

14. A method for fabricating a semiconductor device, as recited in claim 10, wherein the interlayer insulating layer has a first etching rate at least five times as high as a second etching rate of the insulating layer.

15. A method for fabricating a MOS transistor in a semiconductor device, the method comprising the steps of:

forming a gate electrode over a semiconductor substrate;

implanting first impurity ions at a low concentration of a first conductivity type, using the gate electrode as a mask, to form a first impurity diffusion layer;

forming first spacers on lateral sides of the gate;

implanting second impurity ions at a low concentration of a second conductivity type, using the gate and first spacers as a mask, to form a second impurity diffusion layer;

forming a second spacers adjacent to the first spacers;

implanting third impurity ions of high concentration of a second conductivity type, using the gate and the first and second spacers as a mask, to form a third impurity diffusion layer; and

annealing and diffusing the impurity diffusion layers to overlap the first diffusion layer with the second diffusion layer.

16. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the first conductivity type is n-type.

17. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of first impurity ions is performed using arsenic with a dose range of about $5x10^{12}$ ions/cm^2 and at an energy range of about 50 keV.

18. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of second impurity ions is performed using boron or BF_3 with a dose range of about $1x10^{13}$ ions/cm^2 and at an energy range of about 20 keV.

19. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of third impurity ions is performed using boron or BF_3 with a dose range of about $5x10^{15}$ ions/cm^2 and at an energy range of about 20 keV.

Abstract of the Disclosure

An improved source/drain junction configuration in a metal-oxide semiconductor transistor is provided, as well as a novel method for fabricating this junction. This configuration employs gate double sidewall spacers in the peripheral region and gate single sidewall spacers in the cell array region. The double sidewall spacers are advantageously formed to suppress the short channel effect, to prevent current leakage, and to reduce sheet resistance. The insulating layer used to form the second spacers in the peripheral region remains in the cell array region and serves as an etching stopper during the etching step of interlayer insulating layer for contact opening formation and also serves as a barrier layer during the step of silicidation formation. As a result the fabrication process of the resulting device is simplified.

Fig. 1A

(Prior Art)

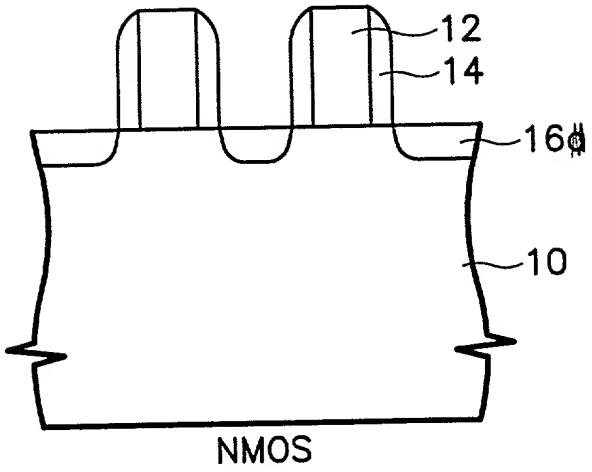


Fig. 1B

(Prior Art)

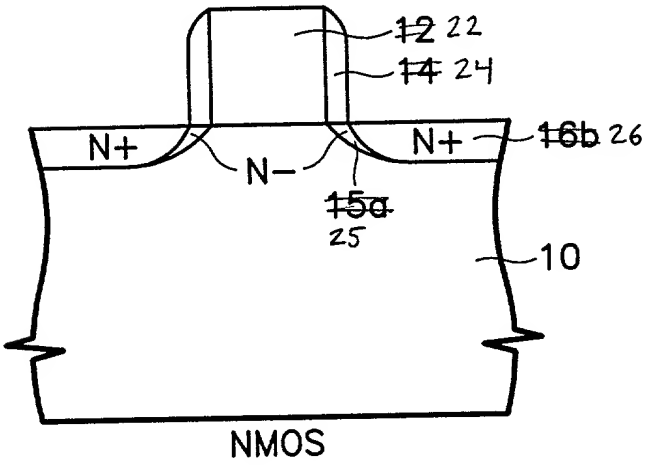


Fig. 1C

(Prior Art)

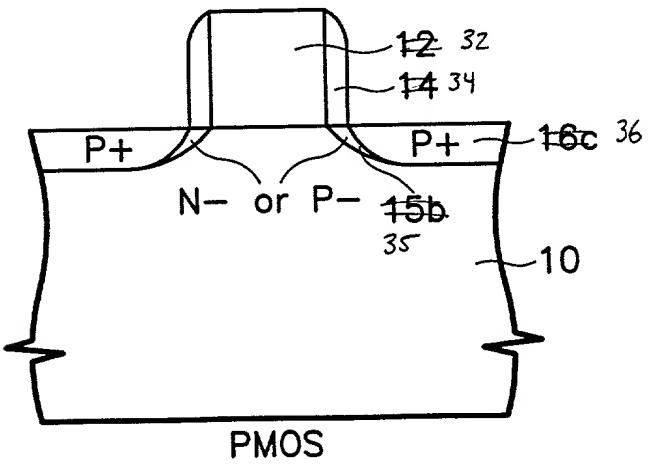


Fig. 2A

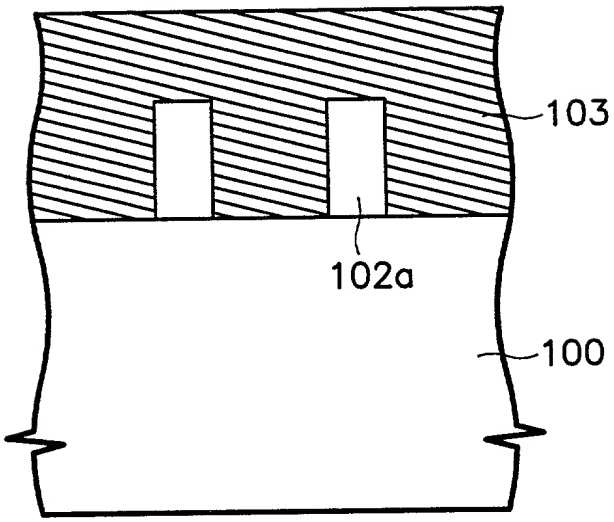


Fig. 2B

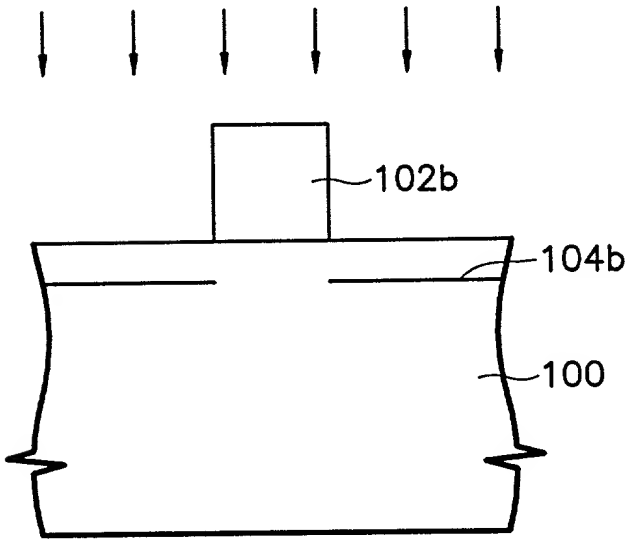


Fig. 2C

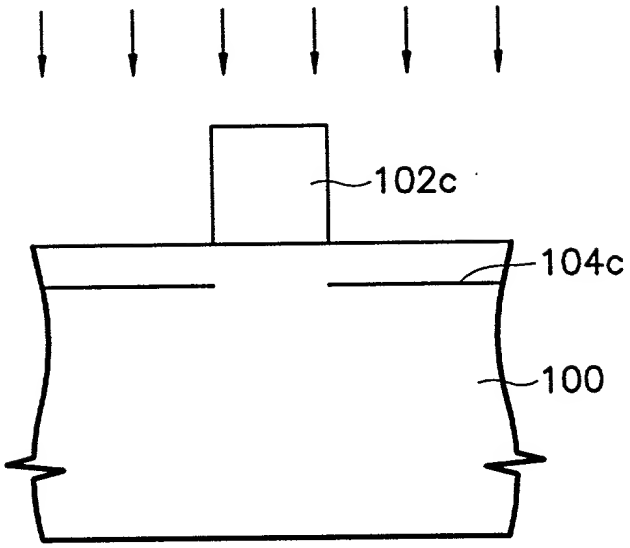


Fig. 3A

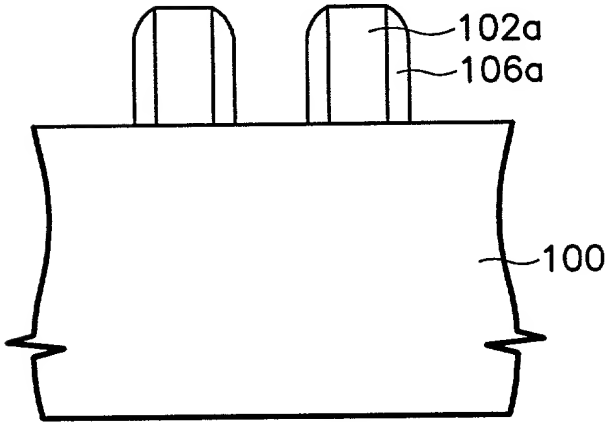


Fig. 3B

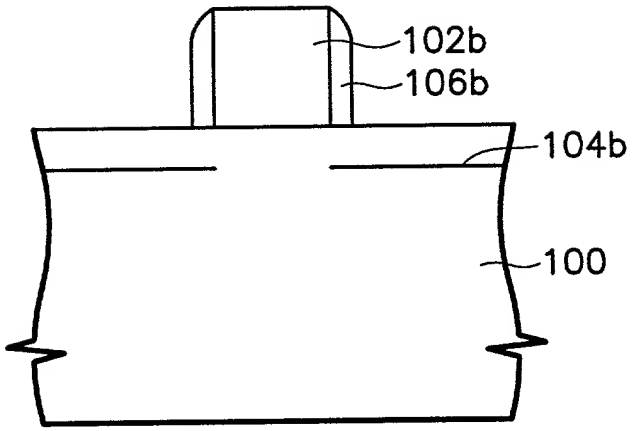


Fig. 3C

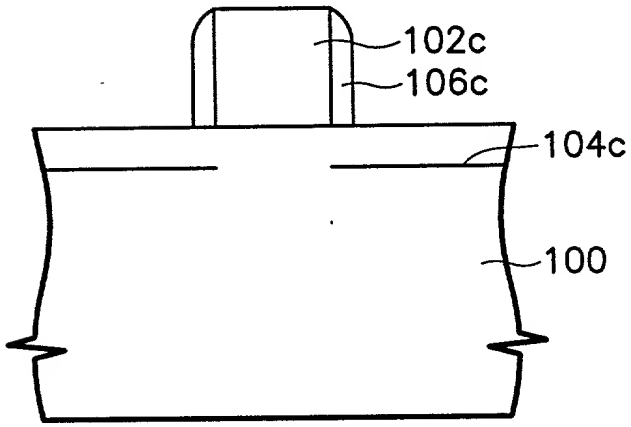


Fig. 4A

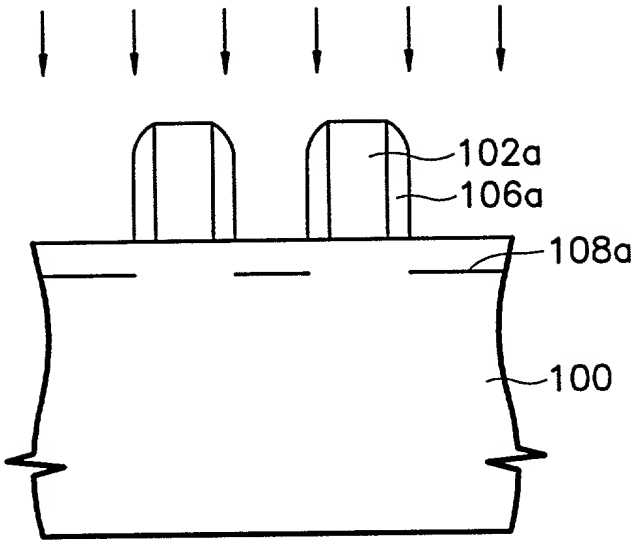


Fig. 4B

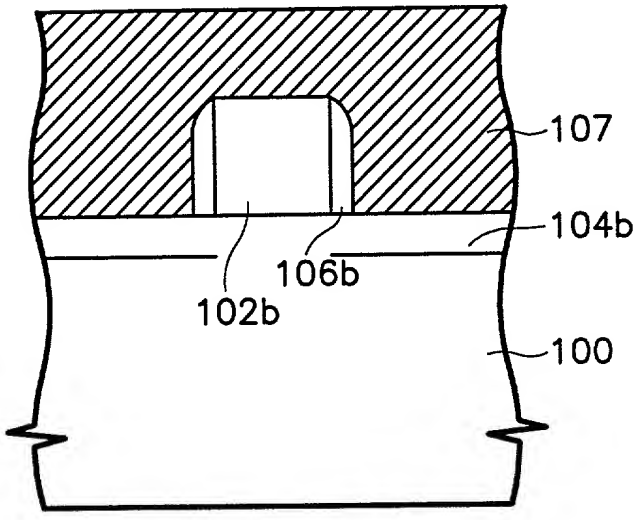


Fig. 4C

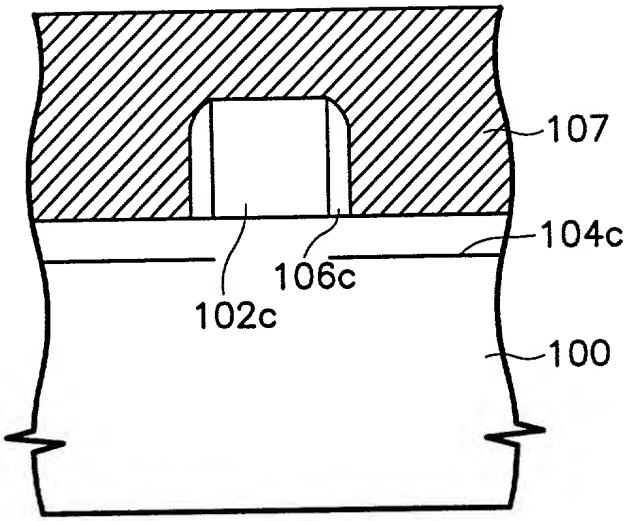


Fig. 5A

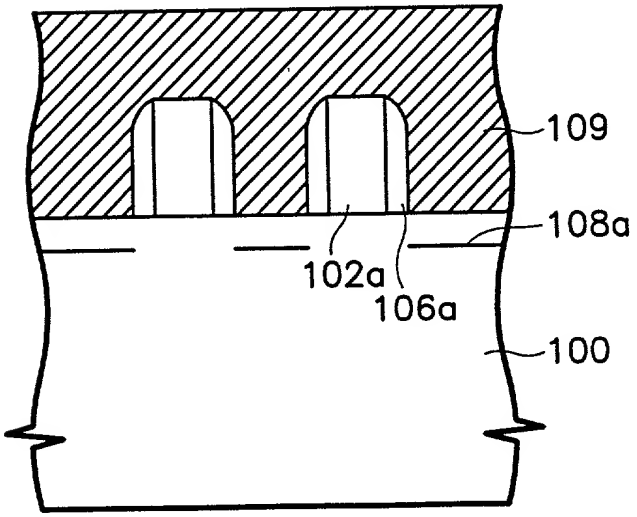


Fig. 5B

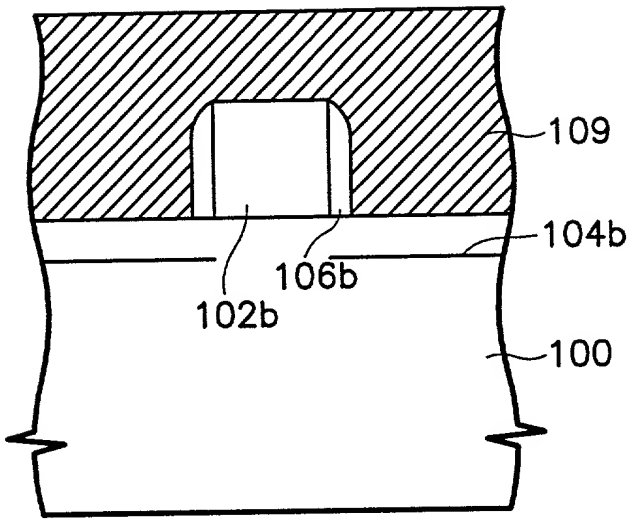


Fig. 5C

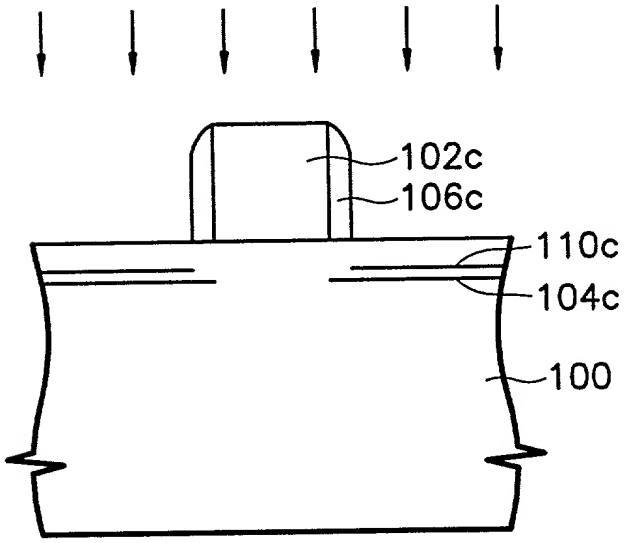


Fig. 6A

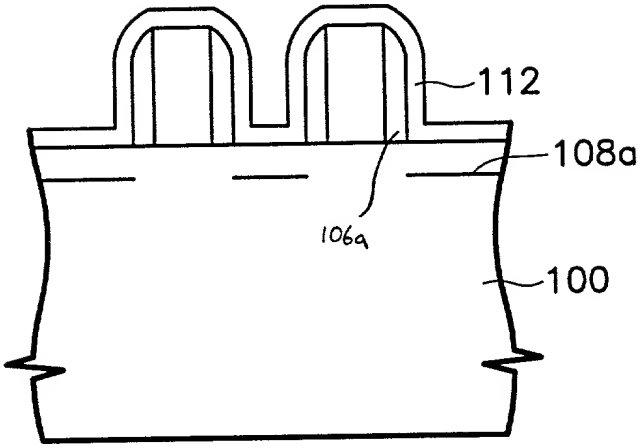


Fig. 6B

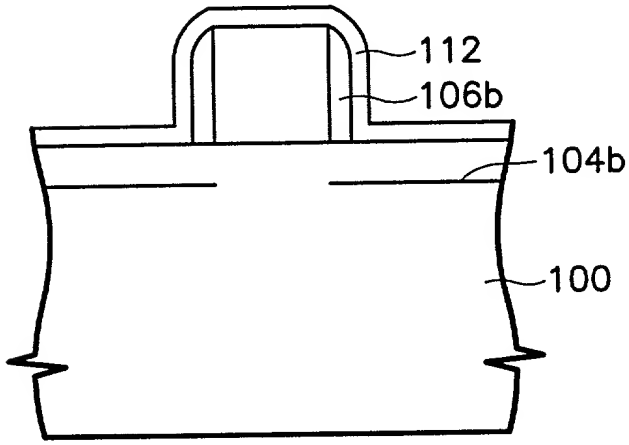


Fig. 6C

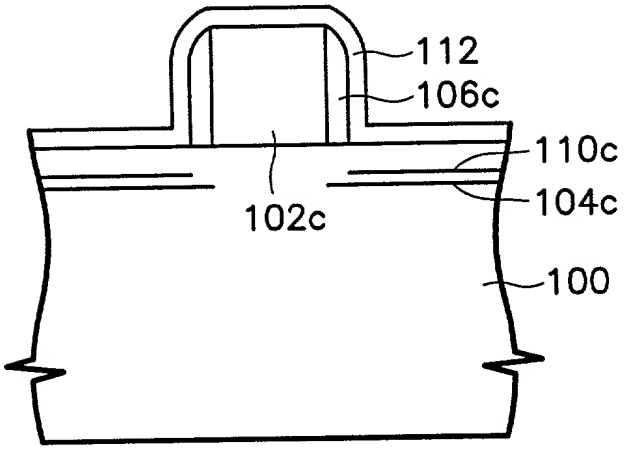


Fig. 7A

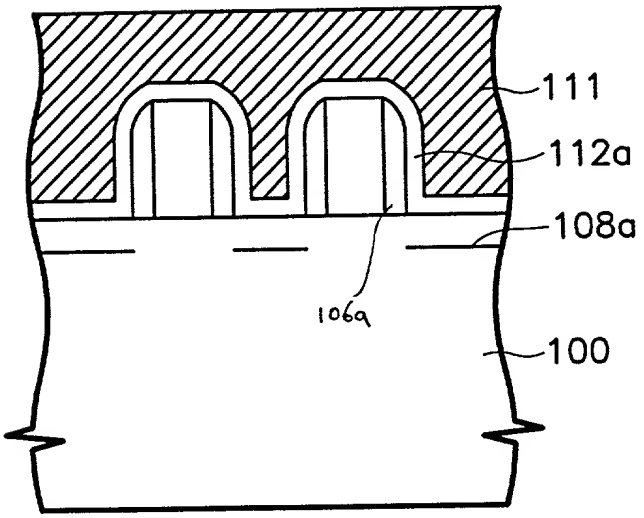


Fig. 7B

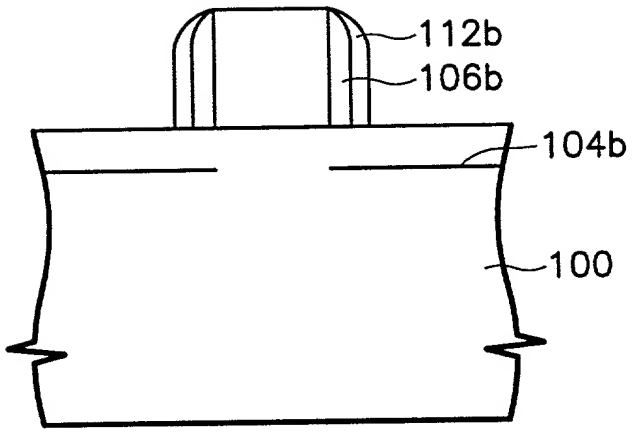


Fig. 7C

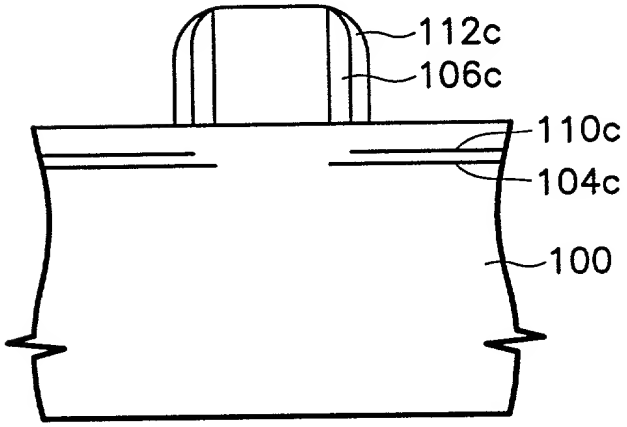


Fig. 8A

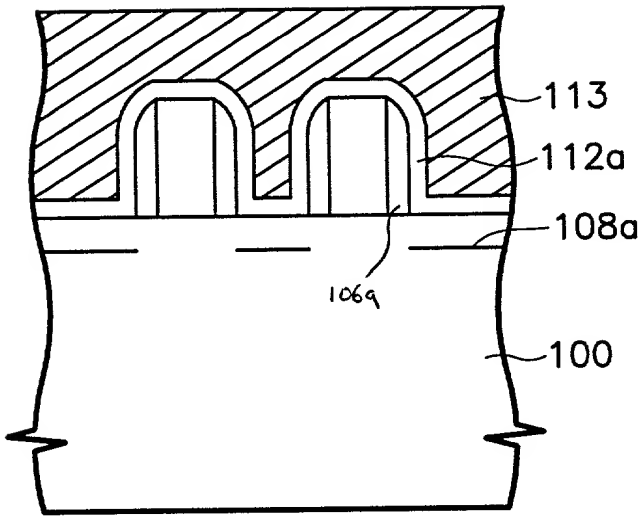


Fig. 8B

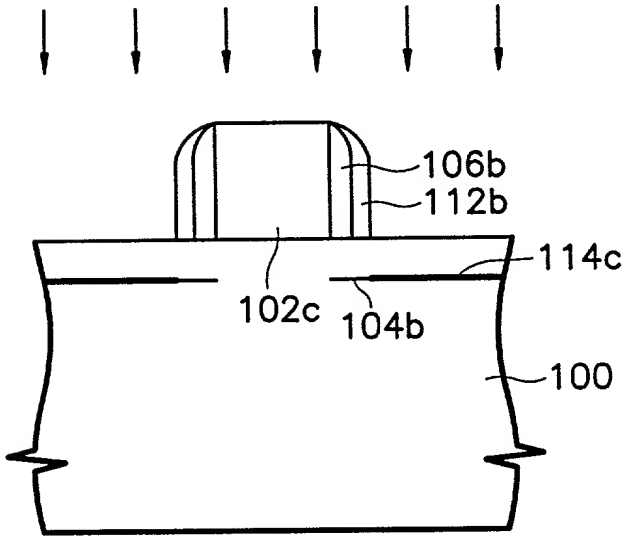


Fig. 8C

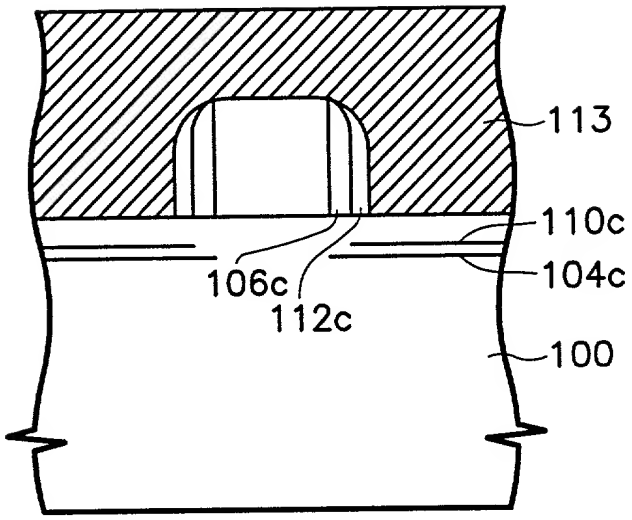


Fig. 9A

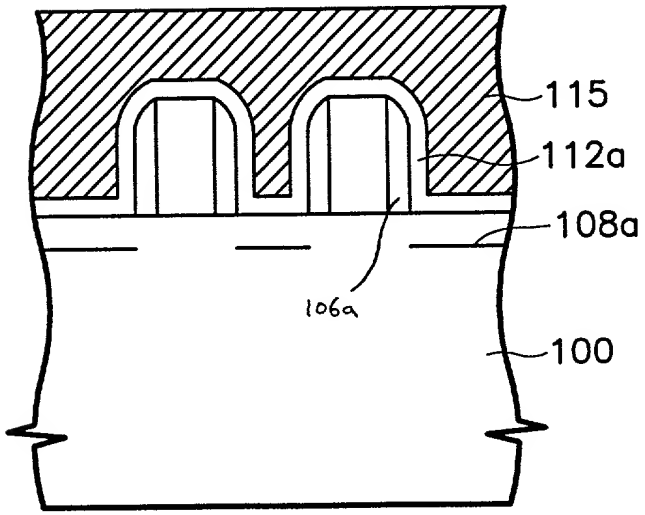


Fig. 9B

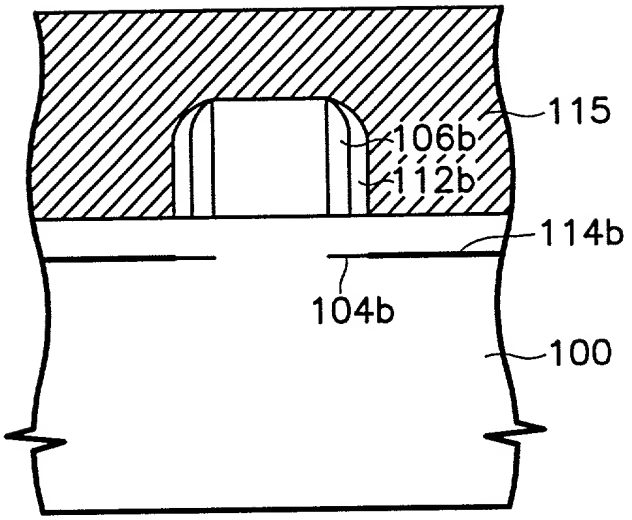


Fig. 9C

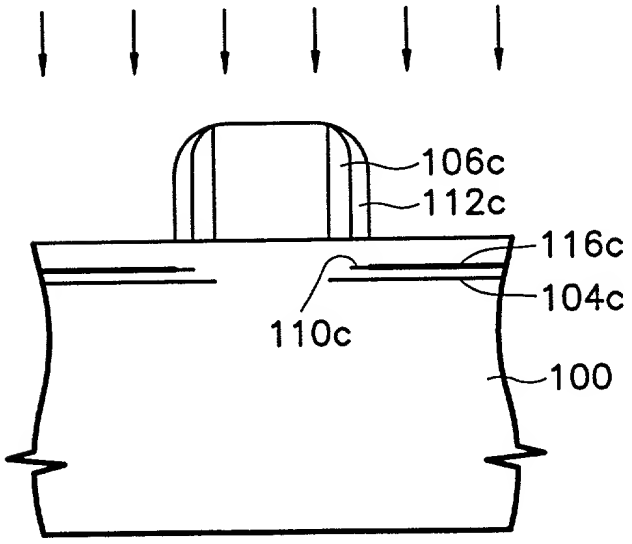


Fig. 10A

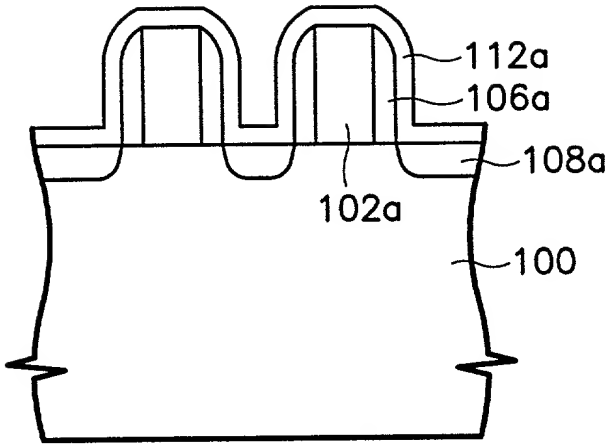


Fig. 10B

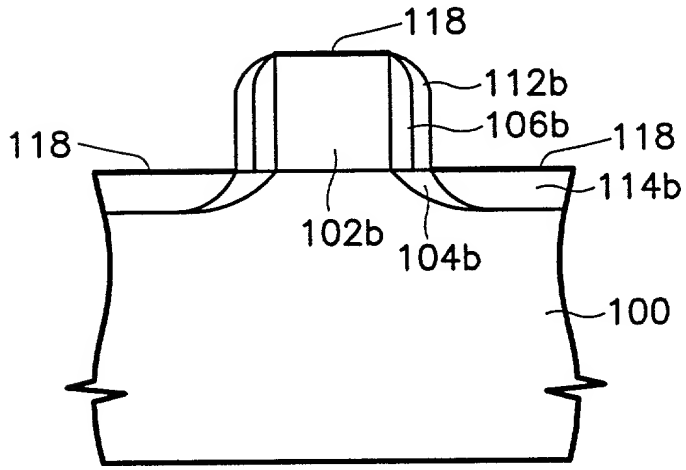


Fig. 10C

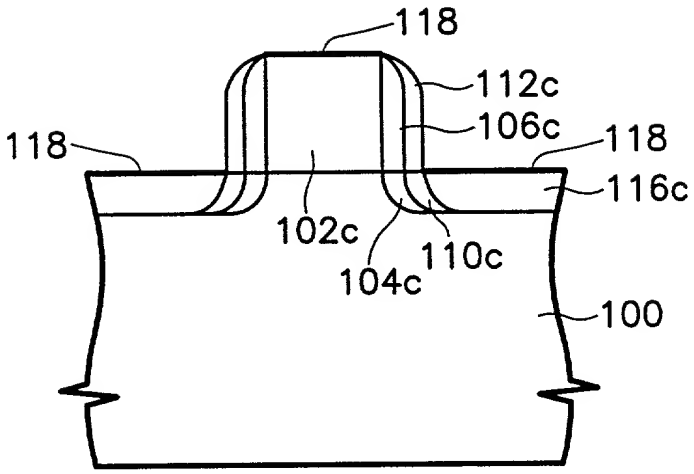


Fig. 11A

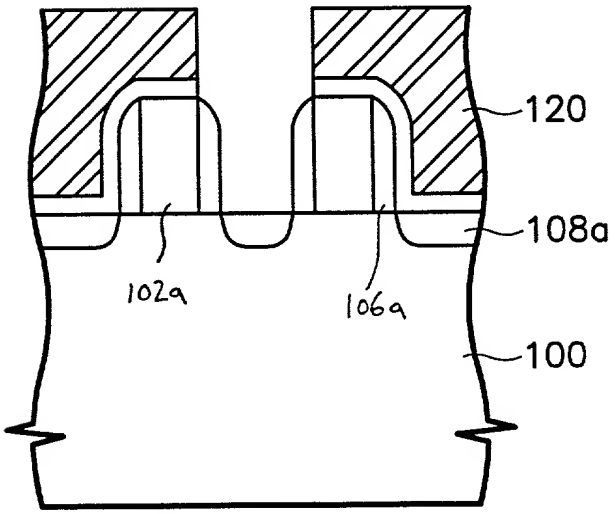


Fig. 11B

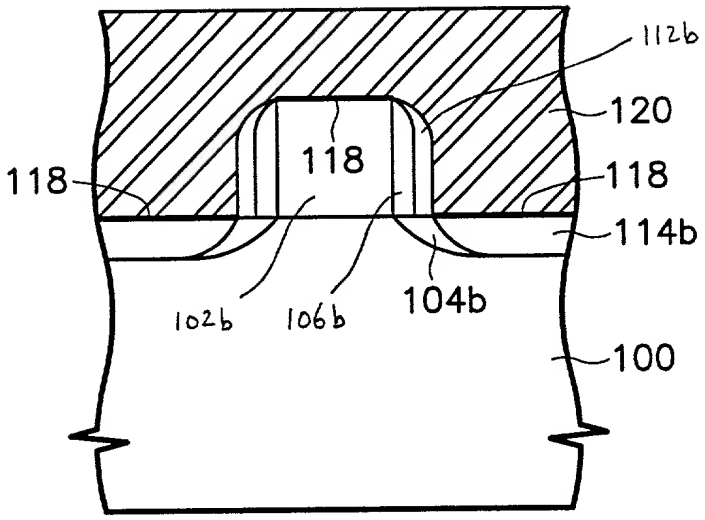
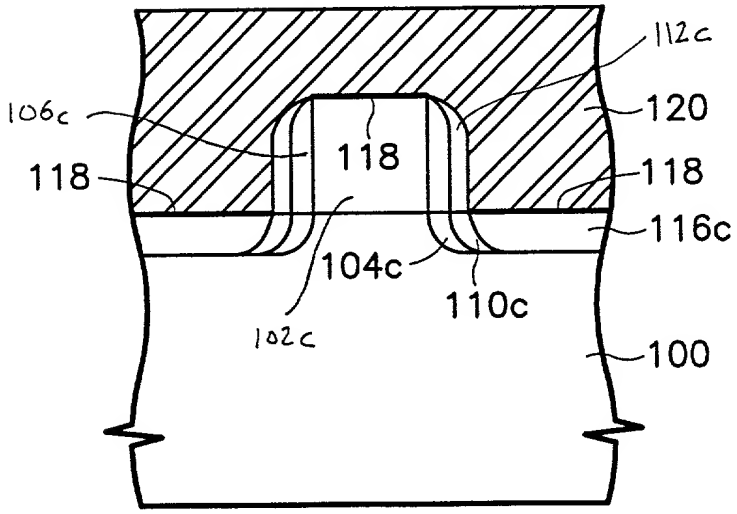


Fig. 11C



JONES & VOLENTINE, L.L.P. (4/99)

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

(x) Original ( ) Supplemental ( ) Substitute ( ) PCT ( ) Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE

of which is described and claimed in:

(x) the attached specification, *or*

( ) the specification in the application Serial No._____ filed_____,

and with amendments through_____ (if applicable), *or*

( ) the specification in International Application No. PCT/_____, filed _____,

and as amended on _____ (if applicable).

I hereby state that I have reviewed and understand the content of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (and §172 if this application is for a Design) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
KOREA	98-18167	May 20, 1998	X

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

And I hereby appoint Raymond C. Jones, Reg. No. 34,631 and Adam C. Volentine, Reg. No. 33,289, members of the firm of JONES & VOLENTINE, L.L.P., jointly and severally, attorneys to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith.

I hereby authorize the U.S. attorneys named herein to accept and follow instructions from HANA INTERNATIONAL PATENT & LAW OFFICE as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and myself. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by me.

Kindly direct all correspondence to: **JONES & VOLENTINE, L.L.P.**
12200 Sunrise Valley Drive
Suite 150
Reston, Virginia 20191

Telephone (703) 715-0870

Full Name of 1st Inventor	FAMILY NAME YANG	FIRST GIVEN NAME Won-Suk	SECOND GIVEN NAME
Residence & Citizenship	CITY Seoul	STATE OR COUNTRY Republic of Korea	COUNTRY OF CITIZENSHIP Republic of Korea
Post Office Address	ADDRESS 1617-10, Seochol-dong, Seocho-ku, Seoul, Republic of Korea	CITY	STATE OR COUNTRY ZIP CODE
Full Name of 2nd Inventor	FAMILY NAME KIM	FIRST GIVEN NAME Ki-Nam	SECOND GIVEN NAME
Residence & Citizenship	CITY Kyunggi-do	STATE OR COUNTRY Republic of Korea	COUNTRY OF CITIZENSHIP Republic of Korea
Post Office Address	ADDRESS 108-502, Life Apt., Kkum town, 932-6, Pyoungchon-dong, Ahnyang-shi, Kyunggi-do, Republic of Korea	CITY	STATE OR COUNTRY ZIP CODE
Full Name of 3rd Inventor	FAMILY NAME CHO	FIRST GIVEN NAME Chang-Hyun	SECOND GIVEN NAME
Residence & Citizenship	CITY Seoul	STATE OR COUNTRY Republic of Korea	COUNTRY OF CITIZENSHIP Republic of Korea
Post Office Address	ADDRESS **9-408, Misung Apt., 17-6, Shincheon-dong, Songpa-ku, Seoul, Republic of Korea**	CITY	STATE OR COUNTRY ZIP CODE

Full Name of 4th Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

Full Name of 5th Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

I further declare that all statements made herein of my own knowledge are true, and that all statements on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1st Inventor Won-Suk YANG Date 22/04/1999
Won-Suk YANG

2nd Inventor Ki Nam KIM Date 03/05/1999
Ki-Nam KIM

3rd Inventor CHANG-HYUN CHO Date 27/04/1999
Chang-Hyun CHO

4th Inventor _____ Date _____

5th Inventor _____ Date _____

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Applicant Reference No.: IE8061-US Atty Docket No.: SEC.636